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Patent

Customer No.: 31561
Docket No.:12423-US-PA-X-0P
Application No.: 10/708,666

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Applicant	: Chung-Chin Shih
Application No.	: 10/708,666
Filed	: 2004/3/18
For	: MEMORY DEVICE AND FABRICATION METHOD THEREOF
Art Unit	: 2811
Examiner	: Douglas W. Owens

Interview Request
002-1-571-273-8300
(Via fax: 1 page)

Examiner Owens,

In the "Response to Arguments" in the Office Action dated October 18, 2005, the Office asserted that the control gate 14 of the select transistor 19 is equivalent to the source line of the instant case. Applicants, however, would like to direct the Office's attention to column 14, line 31-38 and Figure 18 of Yaegashi, which specifically teaches the source line is the conductive material that is formed in the contact hole 26 between the select transistors and above the select transistors 19 and the memory cell transistors 18. Accordingly, the source line of Yaegashi can not be the control gate of the select transistor 19. Moreover, as clearly illustrated in Figure 18, the source line of Yaegashi is disposed vertically or perpendicularly to the select transistors and the memory cell transistors.

If necessary & possible, I can discuss in detail with you regarding the abovementioned issues via a telephonic interview. I may be contacted through email at Belinda@jcipgroup.com.tw.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date: Jan 4, 2006

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